REMARKS/ARGUMENTS

Claims 1, 7-9, 12, and 13 remain pending. Claims 1 and 9 have been amended herein. Claims 2, 6 and 10 have been cancelled herein.

Applicants respectfully requests reconsideration in light of the following remarks.

CLAIMS REJECTION

Rejection of Claims 1-2 and 9-10 under 35 U.S.C. 103(a)

Claim 1-2 and 9-10 in so far as understood, rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Fig. 1 Prior Art, in view of Nakano (US 6147923). Applicant respectfully submits that such rejection is improper for the following reasons:

The applicant's Fig. 1 Prior Art discloses a memory pumping circuit comprising:
A MOS capacitor 12 which is a charging capacitor;
Current source 11;
Node between current source 11 and MOS capacitor 12 providing a pumping voltage VPP as a voltage source for a word line; and
Driving circuit comprising inverter 13 which generates the clock signal θ_2 for pumping the voltage VPP up to meet the high voltage for the word line need.

The memory pumping circuit of the applicant's Fig. 1 Prior Art operates well with the memory operation voltage Vdd=2.5V; but in the case of low power memories such as DRAM or 1T-SRAM in which the operation voltage is limited to 1.8V, the driving current will not guarantee these low power memories working on the normal operation. If increasing the MOS capacitor area to make sure the driving current enough for the VPP output, the manufacture cost will be also increased.

In the Fig. 2(A), the applicant discloses a memory pumping circuit which replaces the MOS capacitor 12 with a DRAM cell capacitor 21. The DRAM cell capacitor 21 comprises a MOS transistor 211 and a Storage Cell 212. The DRAM cell can be manufactured by current DRAM process, and the capacitance of DRAM cell is higher than the MOS capacitor at the same size ($C_{DRAM\_Cell} > 50^* C_{MOS}$). Thus, applicant respectfully submits that, the MOS transistor 211 in Fig. 2(A) considered as a decoupling capacitor and the applicant's invention is considered as adding a decoupling capacitor in series with a capacitor is not appropriate.

Nakano discloses a voltage boosting circuit 10A in Fig. 1 for providing the boosted voltage VOUT to the word line of a memory device including:

A pumping-up circuit comprising an NMOS capacitor 13 and a PMOS capacitor 18 connected in series between to boosted voltage COUT and the output VE of inverter circuit 32.

As description above, applicant discloses a memory pumping circuit which replaces the MOS capacitor with a DRAM cell capacitor. The DRAM cell capacitor comprises a MOS transistor and a Storage Cell, which is not the NMOS capacitor and PMOS capacitor of Nakano. Applicant respectfully submits that, the DRAM cell has higher capacitance than the MOS capacitor, which is not disclosed in Nakano.

Moreover, applicant discloses "The plate end of the storage cell 212 connects to the output port of a driving circuit (Inverter 13) for receiving the clock signal θ_2 to drive the memory capacitor 21. the clock signal θ_1 is input to the inverter 13 to generate the clock signal θ_2. The other plate end of the storage cell 212 connects to MOS transistor 211. The drain, source and gate of the MOS transistor 211 connect together with the current source 11 for charging and providing the pumping voltage VPP"[0003]. Also, the applicant discloses in the Fig. 1 prior art, "The NMOS capacitor 12 is the charging capacitor. The current source 11 of NMOS is used to provide the charge current. A clock signal θ_1 is input to the inverter 13 to generate the clock signal θ_2 for pumping the voltage VPP up to meet the high voltage for the word line need"[0024], wherein the voltage VPP is pumped up following the rising and falling of clock signal θ_2. The applicant discloses that in the case of low power DRAM or 1T-SRAM, the operation voltage Vdd is lower than the VPP output. Thus the voltage VPP is pumped up from the operation voltage Vdd to the world line output needed VPP following the rising and falling of clock signal θ_2.

In comparison, Nakano disclosed that in the initial state, the middle point voltage control circuit 20 drives the middle point voltage VM to 0V and only the end point voltage control inverter 30 drives both NMOS capacitor 13 and PMOS capacitor 18 to the on-state to boost VOUT up to VCC. In the boosting VOUT state, Nakano disclosed "in response to the fall of the address transition detection signal AT, the control signal *BIN goes low, and the PMOS transistor 21 is turned on, whereby the voltage VM is raised from $-\alpha \cdot$ VCC to almost VCC. Meanwhile, since the PMOS capacitor 18 is turned off between the source and the drain thereof, the capacity C2 is reduced, that is, the capacitive load to be driven by the circuit 20 is reduced, whereby the raising of the voltage VM becomes faster than in the case where a normal capacitor is used in place of the PMOS capacitor 18. Following up this raising of the voltage VM, the voltage VOUT is boosted by approximately

(1+α)VCC to be VOUT≈VCC(2+α) with the diode 11 being off."(column 5 lines 30 - lines 43) Thus the voltage VOUT is pumped up from VCC to VCC(2+α) following the address transition detection signal AT. After the voltage VOUT is pumped up, Nakano disclosed "In order to return to the initial state before the next pulse of the address transition detection signal AT comes, both the control signals AIN and *BIN are returned to high, whereby the NMOS transistor 23 is turned on, the PMOS transistor 21 is turned off, and the voltage VM is dropped from VCC to 0V."(column 5 lines 45 – lines 50) In conclusion, the Nakano disclosed a voltage boosting circuit with two control circuits 20 and 30. Without the control circuit 20, the circuit of Nakano cannot pump up a voltage in the circuit from operation voltage to the world line needed voltage. The applicant's invention uses only one inverter 13 to drive the memory capacitor 21.Thus, the Nakano did not disclose the applicant's invention. Applicant respectfully submits that, the applicant's Fig. 1 prior art uses only one inverter 13 to drive the MOS capacitor 12. Therefore it is doubtful about the enablement of the citation combination, applicant's Fig. 1 prior art, in view of Nakano.

Thus the citation, applicant's Fig. 1 prior art, in view of Nakano, is not able to provide a memory pumping circuit which replaces the MOS capacitor with a DRAM cell capacitor, in the prior art neither applicant's Fig. 1 nor Nakano teach and imply using the DRAM cell as capacitor. Therefore, the citations do not teach or suggest all the claim limitations. According to MPEP §2143, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teaching. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or reference when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Rejection of Claims 6-8 and 12-13 under 35 U.S.C. 103(a)

Claim 6-8 and 12-13 in so far as understood, rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Fig. 1 Prior Art, in view of Nakano (US 6147923), and further in view of Hiratsuka et al.(US 5453707). Applicant respectfully submits that such rejection is improper for the following reasons:

Hiratsuka et al. disclosed that a CMOS inverter 18 consists of PMOS transistor Mp1 and NMOS transistor Mn1 to generate first clock signal 01 according to second clock signal at the output of NAAD gate 12 and third clock signal at the output NOR gate 13

having different phases with each other.

However, as the description above, the combination of Applicant's Fig. 1 Prior Art and Nakano cannot provide a memory pumping circuit which replaces the MOS capacitor with a DRAM cell capacitor, where Hiratsuka et al. cannot provide such a pumping circuit either. Moreover, the Nakano disclosed a voltage boosting circuit with two control circuits 20 and 30. The applicant's Fig. 1 prior art uses only one inverter 13 to drive the MOS capacitor 12. Therefore it is doubtful about the enablement of the citation combination, applicant's Fig. 1 prior art, in view of Nakano.

Thus the citation, applicant's Fig. 1 prior art, in view of Nakano, further in view of Hiratsuka et al., is not able to provide a memory pumping circuit which replaces the MOS capacitor with a DRAM cell capacitor. The citations do not teach or suggest all the claim limitations.

Conclusion

In the light of the above remarks, Applicant respectfully submits those pending Claims 1, 7-9, 12 and 13 as currently presented are in condition for allowance. Applicant has thoroughly reviewed that art cited but relied upon by the Examiner. Applicant has concluded that this cited reference do not affect the patentability of these claims as currently presented. Accordingly, reconsideration is respectfully requested.

Respectfully submitted,
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